

EVMINIREV1.2

EVMINI1.2

EvaluationKit

Revision0.9

July9,1998

Thisdocumentispreliminaryandis
subjecttochangewithoutnotice

STMicroelectronics

TechnoparcduPaysdeGex-B.P.112
165,rueEdouarddeBranly
01630SaintGenisPouilly(France)

Table of Contents

1	Motherboard Functional Specifications	1
1.1	EVMI Ntaglance	1
1.2	Unified Memory Architecture	3
1.3	STPCCPU Core	3
1.4	STP CIntegrated Chipset Functions.....	3
1.5	Memory Interface	4
1.6	PC Ibus interface.....	4
1.7	ISA bus interface	5
1.8	Super I/O.....	5
1.9	EIDE	5
1.10	Graphics	5
1.11	Video features	6
2	Hardware Installation	7
2.1	Jumpers	7
2.2	Jumpers location	8
2.3	Installation	11
3	Software Installation.....	15
3.1	Windows 3.1 driver installation	16
3.2	Windows 95 driver installation.....	16
4	Motherboard Hardware Specifications	16
4.1	Connectors	16
4.2	Schematics	28
4.3	Bill of Materials	44
4.4	How to design for both PC Client and PC Consumer.....	56
4.5	PCB	62
4.6	Electrical Specifications	69
5	Motherboard Software Specifications	69
5.1	System Address Map	70
5.2	Interrupts and DMA Channels	72
6	Document History	73

ListofTables

TABLE1.	BlockDiagram	2
TABLE2.	Defaultjumpersetting	10
TABLE3.	SIMMModuleconfigurations.....	11
TABLE4.	J23,J24,J25settings	12
TABLE5.	Bank0setting.....	13
TABLE6.	Bank1 setting.....	13
TABLE7.	Bank2setting.....	13
TABLE8.	Bank3setting.....	13
TABLE9.	J98setting.....	14
TABLE10.	J3setting.....	14
TABLE11.	ConnectorList	17
TABLE12.	ISAConectorPinDefinition(PA1/PB1,PA2/PB2,PA3/PB3).....	18
TABLE13.	Y-CVideoOutputConnectorPinDefinition(U14)	19
TABLE14.	StandardVGAConnectorPinDefinition(P1).....	19
TABLE15.	MouseConnectorPinDefinition(P2).....	20
TABLE16.	KeyboardConnectorPinDefinition(P3).....	20
TABLE17.	VideoInputConnectorPinDefinition(P4)	20
TABLE18.	ParallelConnectorPinDefinition(P5)	21
TABLE19.	CVBSVideoOutputConnectorPinDefinition(P6)	21
TABLE20.	SCARTConnectorPinDefinition(P7).....	22
TABLE21.	PCIConectorPinDefinition(P8,P9,P10).....	22
TABLE22.	PCIConectorPinDefinition(P8)	24
TABLE23.	PCIConectorPinDefinition(P9)	24
TABLE24.	PCIConectorPinDefinition(P10)	24
TABLE25.	COM(SerialPort)ConnectorPinDefinition(P11,P12).....	25
TABLE26.	IDEConnectorPinDefinition(P13,P14).....	25
TABLE27.	FloppyConnectorPinDefinition(P15)	26
TABLE28.	ATXPowerSupplyConnectorPinDefinition(P17).....	26
TABLE29.	Key_LockConnectorPinDefinition(P18).....	27
TABLE30.	ATPowerSupplyConnectorPinDefinition(P19).....	27
TABLE31.	TurboConnectorDefinition(J18).....	27
TABLE32.	HardDriveLedConnectorPinDefinition(J19)	28
TABLE33.	ResetConnectorPinDefinition(J20)	28
TABLE34.	ResetConnectorPinDefinition(J21)	28
TABLE35.	CMOSResetJumperPinDefinition(J92).....	28
TABLE36.	STPCCClient-PoweronstrapuseonEVMINI1.2board	43
TABLE37.	STPCCClientandSTPCCConsumerfunctionnaldifferences.....	57
TABLE38.	STPCCClientandSTPCCConsumerpinoutdifferences	57
TABLE39.	Possiblechoiceswhenmultiplexingsignals	59
TABLE40.	SolutionusingnullresistorsasmultiplexorsandmultipleBOMs.....	60
TABLE41.	PowerSupplyCharacteristics.....	70
TABLE42.	MemoryAddressMap.....	71
TABLE43.	IOAddressMap	72
TABLE44.	IRQChannels	73
TABLE45.	DMACHannels.....	73

1. Motherboard Functional Specifications

The EVMINI 1.2 system board is a high-performance personal computer system board based on a STPC Client microprocessor (or STPC Consumer) running with an external clock of 14.31818 MHz.

This system board integrates an IDE controller, two serial ports, one parallel port as well as keyboard and PS2 type mouse interface. This is controlled by the PC87306-IBE/VUL Super I/O Circuit.

1.1 EVMINI at a glance

STPC:

- Supports socketted DX-66, DX-75, DX2-100, or DX2-120 STPC Client.

Cachememory:

- Integrated L1 writeback cache.
- No L2 cache subsystem can be installed.

Mainmemory :

- Supports four 64-bit memory banks using four single-sided or double-sided 72-pin SIMM modules.

Slots:

- 3x 32-bit PCI Bus slots.
- 3x 16-bit ISA slots

Interfaces:

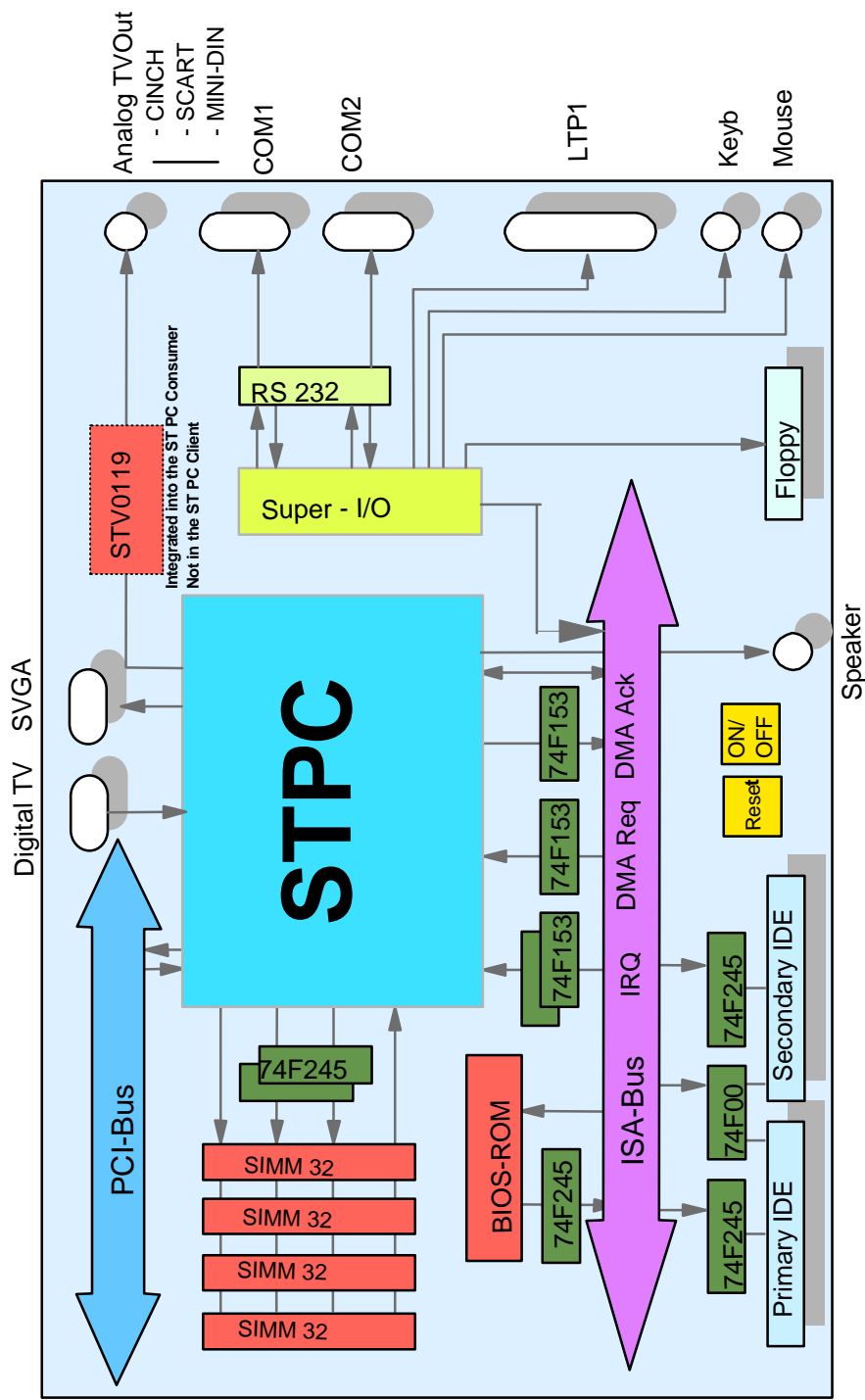
- AT and ATX power supply.
- Keyboard, Mouse, one parallel, two serials.
- Floppy, IDE master, IDE slave.
- VGA monitor.
- CVBS, Y-C, RGB video outputs, Standard Video Input Port.
- Speaker, Reset button, ATX Power Switch button.

Dimensions: 17.5cm x 30.5cm x 6 layers PCB.

Mounting:

10 mounting holes in ATX format

Table1.:BlockDiagram



1.2 UnifiedMemoryArchitecture

TheSTPCchipsarebuiltaroundUnifiedMemoryArchitecture. Thatisthesame64bit wide array of the mother board chip set that are merged with those of advanced accelerating graphics controller by sharing. This approach reduces cost and increases performance. The major advantage of using main memory for the graphic bloc of frame buffer is lower cost (the memory is a low cost commodity DRAM) and the ability to allocate whatever memory you need to graphics without wasting memory. In using 8bit color an 800x600 display requires 470KB of memory and a 1024x768 display requires 768KB of memory but the limitations in available DRAM sizes virtually force the manufacturers to use 1MB frame buffers with consequent waste of memory. From the point of view of performance, the 64-bit wide memory array provides the system with a 200MB/s bandwidth compared with the 100MB/s bandwidth of a typical 32-bit wide memory. The 64-bit wide memory is very helpful on the graphic side because higher bandwidth allows larger screens and greater color depth.

1.3 STPCCPUCore

TheCPUCoreisanST486devicethatrunupto75MHzinDXmode,or120MHzinDX2 mode. The 8k Byte cache can be configured to run in traditional write-through mode or in the higher performance write-back mode. The Floating Point Unit (FPU) is included in the core allowing parallel processing of floating point instructions.

System Management Mode (SMM) provides an additional interrupt and address space that can be used for system power management or software transparent emulation of IO peripherals. While running in isolated SMM address space, the SMM interrupt routine can execute without interfering with the operating system or application programs.

Further power management facilities include a suspend mode that can be initiated from either hardware or software resulting in a power consumption figure < 0.5mA. Because of the static nature of the core, no internal data is lost.

1.4 STPCIntegratedChipsetFunctions

- Two 8237/AT compatible 7-channel DMA controller
- Two 8259/AT compatible interrupt Controller. 16 interrupt inputs-ISA and PCI.
- Three 8254 compatible Timer/Counters.
- Coprocessor Error support logic.
- Power Management and clock/reset unit
- Programmable system activity detector
- Support for STSMI & SMM
- Supports SUSP#
- Slow system clock down to 8MHz
- Slow Host clock down to 8Hz
- Slow graphic clock down to 8Hz
- Supports I/O trap & restart
- Supports APM

- Independent peripheral time-out timer to monitor video, disks, serial and parallel ports.
- Supports RTC, interrupts and DMA wakeup
- 128K SMM_RAM address space from 0xA0000 to 0xB0000
- Supports General purpose I/O's

1.5 Memory Interface

The STPCCL client implements a 64-bit single memory subsystem for both the system as well as the frame buffer memory. In other words, the size of the DRAM available to the system is reduced by the size of the DRAM allocated to the frame buffer.

Here below are listed the major features of the memory controller:

- Integrated system memory and graphic memory.
- Supports up to 128 MBytes system memory in 4 banks.
- Supports 256 KB up to 32 MB single-sided and double-sided DRAM SIMMs.
- Four Double-word write buffers for CPU to DRAM and PCI to DRAM cycles.
- Four Double-word read prefetch buffers for PCI masters.
- Supports Fast Page Mode EDODRAM.
- Programmable timing for DRAM parameters including CAS pulse width, CAS pre-charge time, and RAS to CAS delay
- Hidden refresh.
- Supports memory hole from 1 MByte up to 8 MByte for PCI/ISA devices.
- Shadow memory support for C, D, E, and F blocks.
- Supports memory remap for unused D and E blocks to top of system memory.

The DRAM banks must be equipped with 72-pin SIMMs. Parity is ignored. Fast Page Mode and EDO are supported.

The rules for supported SIMM combinations are:

- If both banks are populated, they are populated with the same amount of memory.
- The lowest numbered bank is filled first.

Although system DRAM data bus is 64-bit wide, 32-bit DRAM bank is also supported by not populating the upper Dword SIMM module for that particular bank but there is a performance degradation due to loss of bandwidth. Graphics and Video features are not functional in that case.

1.6 PCI bus interface

- 3 PCI slots fully compliant with PCI version 2.1 specifications.
- Integrated PCI arbitration interface (32 bit wide, 5V).
- Translation of PCI cycle to ISA bus.
- Translation of ISA master initiated cycle to PCI.
- Support for burst read/write from PCI master.

- 1/3x and 1/2x STPC clock PC I clock.
- The STPC occupies Device number 0 slot on the PCI bus.

1.7 ISA bus interface

- 3 full ISA extension connector.
- The STPC generates the ISA clock from External 14.318 Mhz oscillator clock.
- Supports programmable extra wait state for ISA cycles.
- Supports I/O recovery time for back to back I/O cycles.
- Fast Gate A20 and Fast reset.
- Supports the single ROM that C, D, or E block shares with F block BIOS ROM.
- Supports flash ROM.
- Supports ISA hidden refresh.

1.8 SuperI/O

Onboard SuperI/O (National PC87306 IBE/VUL) provides:

- a PC-AT keyboard interface on mini DIN6 connector.
- a PS/2 mouse interface on mini DIN6 connector.
- a floppy disk interface on 34-pin connector.
- COM1 & COM2 on 9-pin connectors.
- a parallel port.
- a fully compatible RTC including Clock registers and Bytes of non-Volatile RAM.

1.9 EIDE

An EIDE (Extended Intelligent Drive Electronics) is provided by the STPC to connect intelligent drives that integrate the controller (HD, CD-ROM etc.). This port supports LBA (Logic Block Addressing) that allows the use of HD larger than 528 MBytes. To enhance the performance, this port supports DMA type of transfers.

1.10 Graphics

Graphics functions are performed by the STPC. The CRT controller supports up to 1280X1024 display resolutions at 75 HZ refresh rates as defined by *VESA Monitor Timing Standard*. The horizontal timing control fields are all VGA compatible. The vertical timings are extended by 1-bit to accommodate above display resolution. The address registers are extended to allow locating the frame buffer anywhere within the first 4 MB of physical main memory. Here below are listed the major features of the graphic controller

- High performance 64-bit windows accelerator.
- Complete backward compatibility to the IBM VGA and SVGA standards.
- Hardware acceleration for Text (generalized bitmap expansion), bitblts and fills.

- 8,16,24and32-bitpixels.
- Upto4MBlonglinearframebuffer.
- TheoutputisananalogRGBformat,InterlacingisNOTsupported

1.11 Videofeatures.

ATVOutputisprovidedbytheSTPC.TheNTSC/PALencoding(conformtotheNTSC/PALtimingspecifications)isdonebyanSTV0118orSTV0119encoderwhenusingaSTPCClient,andbytheintegratedSTV0119whenusingaSTPCConsumer.Threeanalog output are simultaneously delivered (RGB, Composite and Luma/Croma SVHS compatible).Inadditiontothis,aVideoInputPortispresentonchip,whichtakesavideo streamandstoretheuncompresseddataonalocalvideobufferbeforedisplayingthefull motion sequences through the TV encoder. The STPC provides the capability to superimposeOnScreenDisplay(OSD).

2. HardwareInstallation

When you install the system board, you must configure components, set jumpers, and attach connectors.

2.1 Jumpers

Jumpers

Jumpers on the system board provide information to your system about installed options and system settings. You need to configure jumpers when you install the CPU or clear CMOS memory.

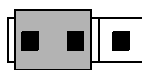
Setting Jumpers

Configures system board option by setting jumper switches.

Note: When you open a jumper, leave the plastic jumper cap attached to one of the pins so you don't lose it.

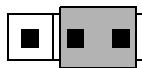
Symbols:

For 3-pin jumpers, the following symbols are used:



123

-Close pins 1 and 2 with a jumper cap.



123

-Close pins 2 and 3 with a jumper cap

For 2-pin jumpers, the following symbols are used:

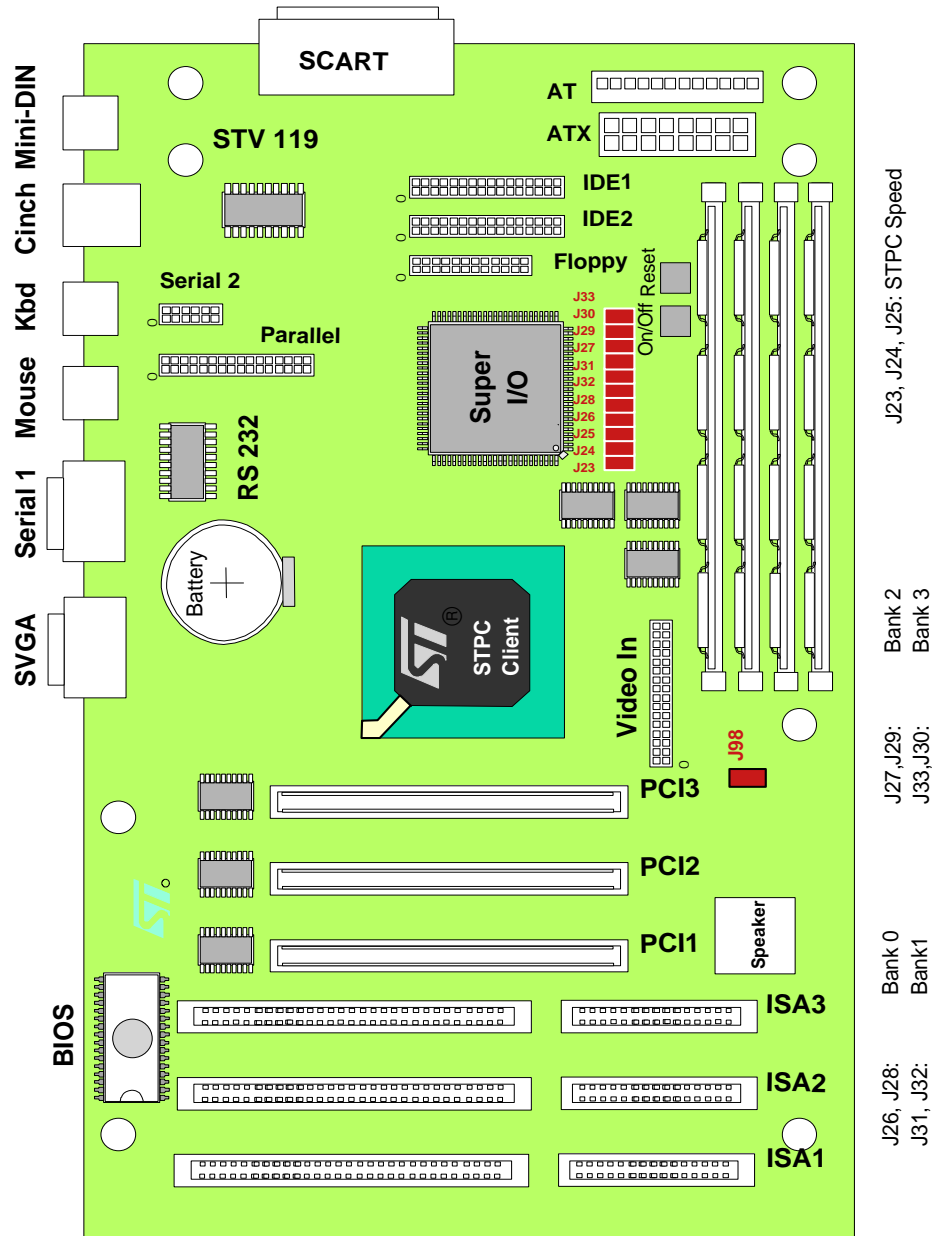


-Close the jumper by inserting the jumper cap over the two pins of the jumper.











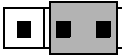
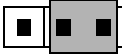












-Open the jumper by inserting the jumper cap over one or no pin(s) of the jumper.

2.2.2 StrapOptions



2.2.3 DefaultJumpersetting.

TABLE2.Defaultjumpersetting

Jumper	Purpose	Setting
J3	TVOutput	
J4,J5,J6,J100	SCARTConfiguration	J4  J5  J6  J100 
J7,J8	SuperI/OBaseAddress	J7  J8 
J92	BackupVoltage	 123
J93	ATXPowerControl	 123
J99	EPROMSize	 123
J23,J24,J25	STPCSpeed	J23  J24  J25 
J98	PCIClockSpeed	
J26,J28	DRAMBank0TypeandSpeed	J26  J28 
J32,J31	DRAMBank1TypeandSpeed	J32  J31 
J27,J29	DRAMBank2TypeandSpeed	J27  J29 
J30,J33	DRAMBank3TypeandSpeed	J30  J33 

2.3 Installation

For mainboard installation, it is important that the jumper settings are set correctly. Improper jumper settings will cause system instability or system hang-ups. Please refer to the installation procedures below.

2.3.1 Step1: Verify STPCC client is correctly inserted on the socket.

STPCC clients should be plugged according to the picture of the board on the cover page. Pin A1 on the device is bottom left on this image: (It corresponds to the arrow designed on the socket)



2.3.2 Step2: Installing the SIMM Modules into the proper SIMM sockets.

This mainboard supports only 4 sockets for memory modules, U8, U9, U10, U11. Bank 0 and Bank 1 (U8, U9) must be populated to have SVGA interface working. The table below lists the possible configurations for U8-U9 and for U10-U11. Using double-sided SIMM modules allow to populate the 4 banks.

TABLE 3. SIMM Module configurations

U8,U9	U10-U11
512Kx32	
1Mx32	512Kx32
2Mx32	1Mx32
4Mx32	2Mx32
8Mx32	4Mx32
16Mx32	8Mx32
	16Mx32

2.3.3 Step3:ClearCMOSmemory.

- Switch off the board
 - SW2 push button for ATX power supply
 - Interruptor on AT power supply
- Place J92 in 2-3 position for 2 seconds and then replace it in 1-2 position (default).

2.3.4 Step4:Use default jumper setting to run BIOS setup.

Power, keyboard, mouse and screen must be correctly connected.
















- Switch on the board.
- Select F2 (BIOS Default Values) when requested on screen.
- Quit saving Configuration.
- Reset the board with SW1 push button.
- Press 'DEL' to launch BIOS SETUP again.
- Goto Setup menu 'Chipset Setup // DRAM Bank 0'.
- Configure DRAM Type and Speed accordingly to plugged memory modules.
- Same for banks 1, 2, and 3.
- Goto Setup menu 'Chipset Setup // DRAM Type / Timing'.
- Select 'User Setup'.
- Quit saving Configuration.

2.3.5 Step5:Setting the STPC Speed Jumper (J23,J24,J25)

Set jumpers J23, J24 and J25 according to the speed of the STPC that is installed. This is validated on reset or Power up. This speed corresponds to HCLK clock. For DX2 devices, CPU core runs at twice this speed.

!Warning: Improper speed setting might cause serious damage to DX2 STPCs.

TABLE 4. J23, J24, J25 settings



Setting	J23	J24	J25
25MHz			
50MHz			
60MHz			
66MHz			
75MHz			

2.3.6 Step6:SettingtheDRAM

Set Jumpers J26, J32, J27 and J30 according to the EDO and FPM Mode DRAM for Bank 0, 1, 2 and 3 respectively.

Set Jumpers J28, J31, J29, and J33 according to the speed of DRAM for Bank 0, 1, 2, and 3 respectively.

Table5.Bank0setting

Setting	J26
FPM	
EDO	





Setting	J28
60ns	
70ns	

Table6.Bank1setting

Setting	J32
FPM	
EDO	





Setting	J31
60ns	
70ns	

Table7.Bank2setting

Setting	J27
FPM	
EDO	







Setting	J29
60ns	
70ns	

Table8.Bank3setting

Setting	J30
FPM	
EDO	



Setting	J33
60ns	
70ns	

Note: You can modify the DRAM Configuration by changing the BIOS setting (The BIOS setting has priority over the jumper setting)

2.3.7 Step7:SettingthePCIClockSpeed(J98)

Set jumper J98 according to STPC speed setup and required PCI clock speed. This is validated on reset or Power up.



TABLE 9. J98 setting

Setting	J98
HCLK/3	
HCLK/2	

2.3.8 Step8:SettingtheRGB/CVBSVideoOutput(J3)

Set jumper J3 according to requested TV Output. SCART connector is configured to generate RGB only. CINCH connector generates CVBS only. Software Installation

TABLE 10. J3 setting

Setting	J3
CVBS	
RGB	

3. SoftwareInstallation

TheEVMINIkiteincludes2floppydisks:

Oneforthewindowsdrivers:

- Windows95Driver
 - GraphicsDriver
 - DirectDrawDriver
 - MCIDriver
- Windows3.1:GraphicsDriver

TheotheroneforEVMINI1.2hardware

- SchematicsoftheboardinORCADandPROTELFormat
- Gerberfilesoftheboard

3.1 Windows3.1driverinstallation

- RunWindowssetup.
- Choose‘ChangeSystemSettings’in‘Option’menu.
- InsertdiskinFloppydrive.
- Select‘Otherdisplay(RequiresdiskfromOEM...’indisplaylist.

3.2 Windows95driverinstallation

- OpenControlPanel.
- SelectDisplayicon.
- SelectSettingsheet.
- Press‘AdvancedProperties’button.
- Press‘Change...’buttoninAdaptersheet.
- InsertdiskinFloppydrive.
- Press‘HaveDisk...’button.
- Press‘OK’.
-
- MotherboardHardwareSpecifications

4. MotherboardHardwareSpecifications

4.1 Connectors

The following table contains the exhaustive list of all the connectors that is implemented on the demo board.

TABLE 11. Connector List

Identification	Name	Type	Nb of Pins
PA1,PA2,PA3	ISA(8-bit)	ISA	62
PB1,PB2,PB3	ISA(16-bit extension)	ISA	36
U14	Y-C Video Output	MiniDin	4
P1	VGA	SubD	15
P2	Mouse	MiniDin	6
P3	Keyboard	MiniDin	6
P4	Video Input	Straight Pinheader	26
P5	Parallel	Straight Pinheader	26
P6	CVBS Video Output	CINCH	1
P7	SCART	SCART	21
P8,P9,P10	PCI	PCI	124
P11	COM	SubD	9
P12	COM	Straight Pinheader	10
P13	IDE-Primary	Straight Pinheader	40
P14	IDE-Secondary	Straight Pinheader	40
P15	Floppy	Straight Pinheader	34
P17	ATX Power Supply	ATX	20
P18	Key_Lock	Straight Pinheader	5
P19	AT Power Supply	AT	12
J18	Turbo	Straight Pinheader	2
J19	HD Led	Straight Pinheader	2
J20	ATX Control	Straight Pinheader	2
J21	Reset	Straight Pinheader	2
J92	CMOS Reset	Straight Pinheader	3

4.1.1 Connector definition

ISA Connectors

TABLE 12. ISA Connector Pin Definition (PA1/PB1, PA2/PB2, PA3/PB3)

Signalname	Pin	Pin	Signalname
GND	B1	A1	IOCHCK#
RSTDRV	B2	A2	SD7
VCC	B3	A3	SD6
IRQ9	B4	A4	SD5
-5V	B5	A5	SD4
DRQ2	B6	A6	SD3
-12V	B7	A7	SD2
0WS	B8	A8	SD1
+12V	B9	A9	SD0
GND	B10	A10	IOCHRDY
SMEMW#	B11	A11	AEN
SMEMR#	B12	A12	SA19
IOW#	B13	A13	SA18
IOR#	B14	A14	SA17
DACK3#	B15	A15	SA16
DREQ3	B16	A16	SA15
DACK1#	B17	A17	SA14
DRQ1	B18	A18	SA13
REFRESH#	B19	A19	SA12
BCLK	B20	A20	SA11
IRQ7	B21	B21	SA10
IRQ6	B22	A22	SA9
IRQ5	B23	A23	SA8
IRQ4	B24	A24	SA7
IRQ3	B25	A25	SA6
DACK2#	B26	A26	SA5
TC	B27	A27	SA4
BALE	B28	A28	SA3
Vcc	B29	A29	SA2
OSC	B30	A30	SA1
GND	B31	A31	SA0
	KEY	KEY	
MEMCS16#	D1	C1	SBHE#
IOCS16#	D2	C2	LA23
IRQ10	D3	C3	LA22
IRQ11	D4	C4	LA21

TABLE12.ISAConnectorPinDefinition(PA1/PB1,PA2/PB2,PA3/PB3)

Signalname	Pin	Pin	Signalname
IRQ12	D5	C5	LA20
IRQ15	D6	C6	LA19
IRQ14	D7	C7	LA18
DACK0#	D8	C8	LA17
DRQ0	D9	C9	MEMR#
DACK5#	D10	C10	MEMW#
DRQ5	D11	C11	SD8
DACK6#	D12	C12	SD9
DRQ6	D13	C13	SD10
DACK7#	D14	C14	SD11
DRQ7	D15	C15	SD12
Vcc	D16	C16	SD13
MASTER#	D17	C17	SD14
GND	D18	C18	SD15

Y-CVideoOutputConnector

TABLE13.Y-CVideoOutputConnectorPinDefinition(U14)

Signalname	Pin
GND	1
GND	2
Y(Luminance)	3
C(Chromanance)	4
GND	5

VGAConnector

TABLE14.StandardVGAConnectorPinDefinition(P1)

SignalName	Pin
Red	1
Green	2
Blue	3
ID2	4
GND	5
GND	6
GND	7
GND	8

TABLE14.StandardVGAConnectorPinDefinition(P1)

SignalName	Pin
VCCFuse	9
GND	10
ID0	11
DDCDAT	12
HS	13
VS	14
DDCCLK	15

MouseConnector**TABLE15.MouseConnectorPinDefinition(P2)**

SignalName	Pin
MData	1
NC	2
GND	3
MVCC	4
MClk	5
NC	6

KeyboardConnector**TABLE16.KeyboardConnectorPinDefinition(P3)**

SignalName	Pin
KBDData	1
NC	2
GND	3
KBVCC	4
KBClk	5
NC	6

VideoInput

TABLE17.VideoInputConnectorPinDefinition(P4)

SignalName	Pin	Pin	SignalName
GND	1	2	D[0]
GND	3	4	D[1]
GND	5	6	D[2]
	7	8	D[3]
	9	10	D[4]
	11	12	D[5]
	13	14	D[6]
	15	16	D[7]
GND	17	18	CLK
GND	19	20	HSYNC
GND	21	22	PARITY
	23	24	
	25	26	GND

ParallelConnectors

TABLE18.ParallelConnectorPinDefinition(P5)

SignalName	Pin	Pin	SignalName
STROBE#1	1	14	AFD#1
DP1_0	2	15	ERROR#1
DP1_1	3	16	INIT#1
DP1_2	4	17	SLCTIN#1
DP1_3	5	18	GND
DP1_4	6	19	GND
DP1_5	7	20	GND
DP1_6	8	21	GND
DP1_7	9	22	GND
ACK#1	10	23	GND
BUSY1	11	24	GND
PE1	12	25	GND
SLCT1	13	26	NC

CVBSVideoOutputConnector

TABLE19.CVBSVideoOutputConnectorPinDefinition(P6)

Signalname	Pin
VIDEO	1
GND	2

SCARTConnectors

TABLE20.SCARTConnectorPinDefinition(P7)

SignalName	Pin	Pin	SignalName
	1	2	
	3	4	GND
GND	5	6	
BLUEOUT	7	8	Pull_Up200/+12V
GND	9	10	
GREENOUT	11	12	
GND	13	14	GND
REDOUT	15	16	Pull_Up82/+5V
GND	17	18	GND
CVBSOUT	19	20	
GND	21		

PCISConnectors

TABLE21.PCIConnectorPinDefinition(P8,P9,P10)

Signalname	Pin	Pin	Signalname
GND	A1	B1	-12V
+12V	A2	B2	NC
NC	A3	B3	GND
NC	A4	B4	NC
Vcc	A5	B5	Vcc
<i>seenext3tables</i>	A6	B6	Vcc
<i>seenext3tables</i>	A7	B7	<i>seenext3tables</i>
Vcc	A8	B8	<i>seenext3tables</i>
Reserved	A9	B9	NC
Vcc	A10	B10	Reserved
Reserved	A11	B11	NC
GND	A12	B12	GND

TABLE21.PCIConnectorPinDefinition(P8,P9,P10)

Signalname	Pin	Pin	Signalname
GND	A13	B13	GND
Reserved	A14	B14	Reserved
RESET#	A15	B15	GND
Vcc	A16	B16	PCICLK
<i>seenext3tables</i>	A17	B17	GND
GND	A18	B18	<i>seenext3tables</i>
Reserved	A19	B19	Vcc
AD30	A20	B20	AD31
3.3V	A21	B21	AD29
AD28	A22	B22	GND
AD26	A23	B23	AD27
GND	A24	B24	AD25
AD24	A25	B25	3.3V
seenext3tables	A26	B26	CBE3#
3.3V	A27	B27	AD23
AD22	A28	B28	GND
AD20	A29	B29	AD21
GND	A30	B30	AD19
AD18	A31	B31	3.3V
AD16	A32	B32	AD17
3.3V	A33	B33	CBE2#
FRAME#	A34	B34	GND
GND	A35	B35	IRDY-
TRDY#	A36	B36	3.3V
GND	A37	B37	DEVSEL#
STOP#	A38	B38	GND
3.3V	A39	B39	PCLOCK#
SDONE	A40	B40	PERR#
SBO#	A41	B41	3.3V
GND	A42	B42	SERR#
PAR	A43	B43	3.3V
AD15	A44	B44	CBE1#
3.3V	A45	B45	AD14
AD13	A46	B46	GND
AD11	A47	B47	AD12
GND	A48	B48	AD10
AD9	A49	B49	GND
KEY	A50	B50	KEY
KEY	A51	B51	KEY

TABLE21.PCIConnectorPinDefinition(P8,P9,P10)

Signalname	Pin	Pin	Signalname
CBE0#	A52	B52	AD8
3.3V	A53	B53	AD7
AD6	A54	B54	3.3V
AD4	A55	B55	AD5
GND	A56	B56	AD3
AD2	A57	B57	GND
AD0	A58	B58	AD1
Vcc	A59	B59	Vcc
NC	A60	B60	NC
Vcc	A61	B61	Vcc
Vcc	A62	B62	Vcc

TABLE22.PCIConnectorPinDefinition(P8)

Signalname	Pin	Pin	Signalname
PCI_INT1#	A6		
PCI_INT3#	A7	B7	PCI_INT2#
		B8	PCI_INT0#
PCI_GNT1#	A17		
		B18	PCI_REQ1#
IDSELB(AD30)	A26		

TABLE23.PCIConnectorPinDefinition(P9)

Signalname	Pin	Pin	Signalname
PCI_INT0#	A6		
PCI_INT2#	A7	B7	PCI_INT1#
		B8	PCI_INT3#
PCI_GNT0#	A17		
		B18	PCI_REQ0#
IDSELA(AD31)	A26		

TABLE24.PCIConnectorPinDefinition(P10)

Signalname	Pin	Pin	Signalname
PCI_INT2#	A6		
PCI_INT0#	A7	B7	PCI_INT3#
		B8	PCI_INT1#
PCI_GNT2#	A17		
		B18	PCI_REQ2#
IDSELC(AD29)	A26		

COM(SerialPort)Connectors

TABLE25.COM(SerialPort)ConnectorPinDefinition(P11,P12)

SignalName	Pin
HD CD#	1
HRxD	2
HTxD	3
HDTR#	4
GND	5
HDSR#	6
HRTS#	7
HCTS#	8
HRI#	9

IDEConnectors

TABLE26.IDEConnectorPinDefinition(P13,P14)

SignalName	Pin	Pin	SignalName
RST#	1	2	GND
HD7	3	4	HD8
HD6	5	6	HD9
HD5	7	8	HD10
HD4	9	10	HD11
HD3	11	12	HD12
HD2	13	14	HD13
HD1	15	16	HD14
HD0	17	18	HD15
GND	19	20	KEY

TABLE26.IDEConnectorPinDefinition(P13,P14)

SignalName	Pin	Pin	SignalName
DREQ	21	22	GND
XIOW#	23	24	GND
XIOR#	25	26	GND
IOCHRDY	27	28	GND
DACK#	29	30	GND
IRQ	31	32	IOCS16#
XA1	33	34	GND
XA0	35	36	XA2
HCS#0	37	38	HCS#1
Activity	39	40	GND

FloppyConnector

TABLE27.FloppyConnectorPinDefinition(P15)

SignalName	Pin	Pin	SignalName
GND	1	2	DENSEL
GND	3	4	Reserved
KEY	5	6	DRATE0
NC	7	8	Index#
GND	9	10	MTR#0
GND	11	12	DDR#1
NC	13	14	DR#0
GND	15	16	MTR#2
MSEN1	17	18	DIR#
GND	19	20	STEP#
GND	21	22	WDATA#
GND	23	24	WGATE#
GND	25	26	TRK0#
MSEN0	27	28	WP#
GND	29	30	RDATA#
GND	31	32	HDSEL
GND	33	34	DSKCHG

ATXPowerSupplyConnectors

TABLE28.ATXPowerS upplyConnectorPinDefinition(P17)

SignalName	Pin	Pin	SignalName
+3.3V	11	1	+3.3V
-12V	12	2	+3.3V
GND	13	3	GND
ON#/OFF	14	4	+5V
GND	15	5	GND
GND	16	6	+5V
GND	17	7	GND
-5V	18	8	POWERGOOD
+5V	19	9	+5VSupplyBackup
+5V	20	10	+12V

Key_LockConnector

TABLE29.Key_LockConnectorPinDefinition(P18)

Signalname	Pin
LED_PWR	1
Key	2
GND	3
KEYLOCK	4
GND	5

ATPowerSupplyConnector

TABLE30.ATPowerS upplyConnectorPinDefinition(P19)

SignalName	Pin
PowerGood	1
+5V	2
+12V	3
-12V	4
GND	5
GND	6
GND	7
GND	8
-5V	9
+5V	10
+5V	11
+5V	12

TurboConnector

TABLE31.TurboConnectorDefinition(J18)

Signalname	Pin
Turbo	1
GND	2

HDLedConnector

TABLE32.HardDriveLedConnectorPinDefinition(J19)

Signalname	Pin
Pull_Up_150	1
HDActive	2

ATXControl

TABLE33.ResetConnectorPinDefinition(J20)

Signalname	Pin
ON/OFF	1
GND	2

ResetConnector

TABLE34.ResetConnectorPinDefinition(J21)

Signalname	Pin
Reset	1
GND	2

CMOSResetJumper

TABLE35.CMOSResetJumperPinDefinition(J92)

Signalname	Pin
Battery	1
VBAT	2
GND	3

TABLE36.STPCCClient-PoweronstrapuseonEVMINI1.2board

Note: Bold and italic lines refer to default settings

Function	Name				Purpose
TVOutput	J3				SelectTVOutputreferencesignal
	open				CVBSOutput
	<i>close</i>				<i>RGBOutput</i>
SCARTCon- figuration	J4	J5	J6	J100	SetVideoOutputonScartConfiguration
	<i>close</i>	<i>open</i>	<i>open</i>	<i>close</i>	<i>RGB/SVHS/CVBSsignals</i>
SuperI/O BaseAddress	J7	J8			BaseAddressselection
	open	open			0x398
	open	close			0x26E
	close	open			0x15C
	<i>close</i>	<i>close</i>			<i>0x2E</i>
BackupVolt- age	J92				CMOSparametersused
	<i>1-2</i>				<i>CurrentCMOSRAMparameters(normaloperation)</i>
	2-3				ForceATXpowersupplyon
ATXpower control	J93				SpecifyATXpowermode
	1-2				forceATXpowersupplyon
	<i>2-3</i>				<i>Switchandsoftwarecontrol</i>
	open				ForceATXpowersupplyoff
EPROMsize	J99				DefinethesizeofBIOSEEPROM
	1-2				1MBytes
	<i>2-3</i>				<i>2MBytes</i>
STPCSPEED	J23	J24	J25		SpecifytheCPUfrequency(HCLK)
	open	open	open		75MHz
	<i>open</i>	<i>open</i>	<i>close</i>		<i>66MHz</i>
	open	close	open		60MHz
	open	close	close		50MHz
	close	open	open		25MHz
	close	open	close		reserved
	close	close	open		reserved
	close	close	close		reserved
PCIClock Speed	J98				SpecifythePCibusfrequency
	open				HCLK/3
	<i>close</i>				<i>HCLK/2</i>
DRAM Bank0Type	J26				Specifythetypeofmemorychipforbank0
	<i>open</i>				<i>FastPageMode(FPM)DRAM</i>
	close				ExtendedDataOut(EDO)DRAM

TABLE36.STPCClient-PoweronstrapuseonEVMINI1.2board

Note: Bold and italic lines refer to default settings

Function	Name				Purpose
DRAM Bank0Speed	J28				Specify the speed of memory chip for Bank0
	open				60ns
	<i>close</i>				<i>70ns</i>
DRAM Bank1Type	J32				Specify the type of memory chip for Bank1
	<i>open</i>				<i>FastPageMode(FPM)DRAM</i>
	close				ExtendedDataOut(EDO)DRAM
DRAM Bank1Speed	J31				Specify the speed of memory chip for Bank1
	open				60ns
	<i>close</i>				<i>70ns</i>
DRAM Bank2Type	J27				Specify the type of memory chip for Bank2
	<i>open</i>				<i>FastPageMode(FPM)DRAM</i>
	close				ExtendedDataOut(EDO)DRAM
DRAM Bank2Speed	J29				Specify the speed of memory chip for Bank2
	open				60ns
	<i>close</i>				<i>70ns</i>
DRAM Bank3Type	J30				Specify the type of memory chip for Bank3
	<i>open</i>				<i>FastPageMode(FPM)DRAM</i>
	close				ExtendedDataOut(EDO)DRAM
DRAM Bank3Speed	J33				Specify the speed of memory chip for Bank3
	open				60ns
	<i>close</i>				<i>70ns</i>

4.3.2 BOMwhenusingSTPCCClient

EVMINI1.2 Client

Revised: May 8, 1998

Revision: 1.2

Bill Of Materials

May 8, 1998

3:18:11

Item	Quantity	Reference	Part
1	1	B1	3.0V COIN
2	10	C1,C144,C145,C146,C147, C148,C149,C150,C151,C152	10nF 0805
3	69	C2,C3,C4,C5,C6,C7,C8,C9, C10,C11,C12,C13,C14,C15, C16,C17,C18,C19,C20,C21, C22,C23,C24,C25,C26,C27, C28,C29,C30,C31,C32,C33, C34,C35,C36,C37,C38,C39, C40,C41,C42,C43,C44,C45, C46,C47,C48,C49,C50,C51, C52,C53,C54,C140,C153, C154,C155,C156,C157,C158, C159,C160,C161,C162,C163, C164,C165,C173,C174	.1uF 0805
4	9	C55,C56,C61,C62,C63,C64, C65,C66,C67	1uF A
5	10	C57,C58,C59,C60,C166, C167,C168,C169,C170,C171	33uF C
6	19	C68,C69,C70,C71,C72,C73, C74,C75,C76,C77,C78,C79, C80,C81,C82,C83,C84,C85, C143	22uF B
7	4	C88,C89	15pF 0805
8	4	C90,C91,C92,C93	220pF 0805
9	4	C94,C95,C96,C97	330pF 0805
10	14	C98,C99,C100,C101,C102, C103,C104,C105,C131,C132, C133,C134,C135,C136	390pF 0805
11	4	C106,C107,C108,C109	3.3nF 0805
12	11	C110,C111,C112,C113,C114, C115,C116,C117,C118,C119, C120	47pF 0805
13	2	C121,C122	680pF 0805
14	8	C123,C124,C125,C126,C127, C128,C129,C130	470pF 0805
15	3	C137,C138,C139	10uF B
16	2	C141,C142	22uF_16V D
17	1	C172	220uF B
18	1	D1	LM385BZ TO92
19	12	D2,D3,D4,D5,D6,D7,D8,D9, D10,D11,D12,D13	1N4148 SOT23
20	4	D14,D15,D16,D17	BAR43 SOT23
21	4	DL1,DL2,DL3,DL4	LED SOT23 *
22	2	FB1,FB2	FBEAD FERRITE
23	1	HP1	SPEAKER
24	24	J1,J3,J4,J5,J6,J7,J8,J18, J19,J20,J21,J23,J24,J25, J26,J27,J28,J29,J30,J31, J32,J33,J98,J100	JUMPER_2X1 HEADER_2X1
25	17	J34,J35,J36,J37,J38,J39, J40,J41,J42,J43,J44,J45, J46,J47,J48,J49,J50	STR3CMS STR3CMS

26	2	J72,J73	TESTPIN HEADER_1X1
27	3	J92,J93,J99	HEADER_3 HEADER_3X1
28	6	L1,L2,L3,L4,L5,L6	BEAD 1206
29	4	L7,L8,L9,L10	2.7uH 1206
30	1	L11	BEAD
31	1	OS1	OSCP OSCP
32	1	OS2	27MHz
33	1	P1	DBS15F DBS15F
34	2	P2,P3	MINIDIN MINIDIN
35	2	P4,P5	HEADER_13X2 HEADER_13X2
36	1	P6	CINCH_F CINCH_F
37	1	P7	PERITEL SCART
38	3	P8,P9,P10	PCI32 PCI32
39	1	P11	CONNECTOR_DB9 DB9MC
40	1	P12	HEADER_5X2 HEADER_5X2
41	2	P13,P14	HEADER_20X2 HEADER_20X2
42	1	P15	HEADER_17X2 HEADER_17X2
43	1	P17	ATX ATX
44	1	P18	HEADER_5 HEADER_5X1
45	1	P19	POWER12 POWER12
46	3	PA1,PA2,PA3	BUS62 BUS62
47	3	PB1,PB2,PB3	BUS36 BUS36
48	4	Q1,Q2,Q3,Q4	2N2907A SOT23
49	2	Q5,Q6	2N3904 SOT23
50	1	Q7	2N3906 SOT23
51	31	R1,R2,R4,R5,R6,R7,R8, R9,R10,R11,R12,R13,R14, R15,R16,R17,R18,R19,R20, R21,R22,R23,R24,R25,R26, R27,R28,R29,R30,R31	33 0805
52	11	R32,R33,R34,R35,R36,R37, R38,R39,R40,R41,R42	1K 0805
53	22	R44,R45,R46,R47,R48,R49, R50,R51,R52,R53,R54,R55, R57,R58,R59,R60,R61,R62, R80,R166,R167	4.7K 0805
54	1	R63	536_1% 0805
55	10	R64,R66,R67,R68,R69,R70, R71,R72,R73,R74	22 0805
56	17	R75,R76,R77,R78,	0 0805
58	7	R93,R94,R95,R96,R97,R98, R99	75_1% 0805
59	14	R100,R101,R102,R103,R104, R105,R106,R107,R108,R109, R110,R111,R112,R170	10K 0805
60	4	R113,R114,R115,R116	200 0805
61	5	R117,R118,R119,R120,R121	1.2K 0805
62	4	R122,R123,R124,R125	12 0805
63	4	R126,R127,R128,R129	1.8K 0805
64	4	R130,R131,R132,R133	8.2 0805
65	1	R134	3.3K 0805
66	7	R135,R136,R137,R138,R139, R140,R175	2.2K 0805
67	4	R141,R142,R143,R144	300 0805
68	1	R145	10M 0805
69	3	R146,R147,R148	100 0805
70	4	R149,R150,R151,R152	82 0805
71	6	R153,R154,R155,R163,R164, R165	150 0805

72	2	R156,R157	5.6K 0805
73	3	R158,R159,R174	220 0805
74	2	R160,R173	330 0805
75	2	R161,R162	8.2K 0805
76	1	R168	200
77	1	R169	82
78	1	R171	0
79	64	RP1A,RP1B,RP1C,RP1D,RP2A,RP2B,RP2C,RP2D,RP3A,RP3B,RP3C,RP3D,RP4A,RP4B,RP4C,RP4D,RP5A,RP5B,RP5C,RP5D,RP6A,RP6B,RP6C,RP6D,RP7A,RP7B,RP7C,RP7D,RP29A,RP29B,RP29C,RP29D,RP30A,RP30B,RP30C,RP30D,RP31A,RP31B,RP31C,RP31D,RP32A,RP32B,RP32C,RP32D,RP33A,RP33B,RP33C,RP33D,RP34A,RP34B,RP34C,RP34D,RP35A,RP35B,RP35C,RP35D,RP36A,RP36B,RP36C,RP36D,RP37A,RP37B,RP37C,RP37D	CRA4 22
80	16	RP8A,RP8B,RP8C,RP8D,RP9A,RP9B,RP9C,RP9D,RP10A,RP10B,RP10C,RP10D,RP11A,RP11B,RP11C,RP11D	CRA4 2.2K
81	32	RP12A,RP12B,RP12C,RP12D,RP13A,RP13B,RP13C,RP13D,RP14A,RP14B,RP14C,RP14D,RP15A,RP15B,RP15C,RP15D,RP16A,RP16B,RP16C,RP16D,RP17A,RP17B,RP17C,RP17D,RP18A,RP18B,RP18C,RP18D,RP21A,RP21B,RP21C,RP21D	CRA4 8.2K
82	8	RP19A,RP19B,RP19C,RP19D,RP20A,RP20B,RP20C,RP20D	CRA4 5.6K
83	42	RP22A,RP22B,RP22C,RP22D,RP23A,RP23B,RP23C,RP23D,RP26A,RP26B,RP26C,RP26D,RP27A,RP27B,RP27C,RP27D,RP38A,RP38B,RP38C,RP38D,RP39A,RP39B,RP39C,RP39D,RP40A,RP40B,RP40C,RP40D,RP41A,RP41B,RP41C,RP41D,RP42,RP43,RP43C,RP43D,RP44A,RP44B,RP44C,RP44D,RP45,RP46	CRA4 4.7K
84	8	RP24A,RP24B,RP24C,RP24D,RP25A,RP25B,RP25C,RP25D	CRA4 330
85	4	RP28A,RP28B,RP28C,RP28D	CRA4 150
86	2	SW1,SW2	SW_PUSHBUTTON SWCI
87	1	U1	SIP1 BGA388
88	6	U2,U3,U4,U5,U6,U7	74F245 SO20
89	4	U8,U9,U10,U11	SIMM-36BIT SIMM72
90	1	U12	STV0119 SO28
91	1	U13	LF33 DPAK
92	1	U14	MINIDIN4 MINIDIN4
93	4	U15,U16,U17,U18	74F153 SO16
94	1	U19	74F138 SO16

95	1	U20	PC87306VUL PQFP160
96	2	U21A,U21D	74F32 SO14
97	4	U22,U23,U24,U25	74F74V SO14
98	1	U26	M27C2001 DIP32
99	1	U27	UM8667 SSOP48
100	4	U28A,U28B,U28C,U28D	74F00 SO14
101	4	U29A,U29B,U29C,U29D	74LS14 SO14
102	1	U30	74F32V SO14
103	1	U31	74LS14V SO14
104	1	U32	LT1085CT TO220
105	1	U33	74F125
106	1	U34	74LS14
108	1	Y2	32KHz KF38

DO NOT INSTALL

Y1

R3,R56,R65,R79,R81,R82,R83,R84,R85,R86,R87,R88,R89,R90,R91,R92

C86,C87

STR3CMS

Assemble all in [1-2] position

WIRING MODIFICATIONS

4.3.3 BOMwhenusingSTPCConsumer

EVMINI1.2 Consumer

Revised: May 8, 1998

Revision: 1.2

Bill Of Materials

May 8, 1998

3:18:11

Item	Quantity	Reference	Part
1	1	B1	3.0V COIN
2	10	C1,C144,C145,C146,C147, C148,C149,C150,C151,C152	10nF 0805
3	69	C2,C3,C4,C5,C6,C7,C8,C9, C10,C11,C12,C13,C14,C15, C16,C17,C18,C19,C20,C21, C22,C23,C24,C25,C26,C27, C28,C29,C30,C31,C32,C33, C34,C35,C36,C37,C38,C39, C40,C41,C42,C43,C44,C45, C46,C47,C48,C49,C50,C51, C52,C53,C54,C140,C153, C154,C155,C156,C157,C158, C159,C160,C161,C162,C163, C164,C165,C173,C174	.1uF 0805
4	9	C55,C56,C61,C62,C63,C64, C65,C66,C67	1uF A
5	10	C57,C58,C59,C60,C166, C167,C168,C169,C170,C171	33uF C
6	19	C68,C69,C70,C71,C72,C73, C74,C75,C76,C77,C78,C79, C80,C81,C82,C83,C84,C85, C143	22uF B
7	4	C86,C87,C88,C89	15pF 0805
8	4	C90,C91,C92,C93	220pF 0805
9	4	C94,C95,C96,C97	330pF 0805
10	14	C98,C99,C100,C101,C102, C103,C104,C105,C131,C132, C133,C134,C135,C136	390pF 0805
11	4	C106,C107,C108,C109	3.3nF 0805
12	11	C110,C111,C112,C113,C114, C115,C116,C117,C118,C119, C120	47pF 0805
13	2	C121,C122	680pF 0805
14	8	C123,C124,C125,C126,C127, C128,C129,C130	470pF 0805
15	3	C137,C138,C139	10uF B
16	2	C141,C142	22uF_16V D
17	1	C172	220uF B
18	1	D1	LM385BZ TO92
19	12	D2,D3,D4,D5,D6,D7,D8,D9, D10,D11,D12,D13	1N4148 SOT23
20	4	D14,D15,D16,D17	BAR43 SOT23
21	4	DL1,DL2,DL3,DL4	LED SOT23 *
22	2	FB1,FB2	FBEAD FERRITE
23	1	HP1	SPEAKER
24	24	J1,J3,J4,J5,J6,J7,J8,J18, J19,J20,J21,J23,J24,J25, J26,J27,J28,J29,J30,J31, J32,J33,J98,J100	JUMPER_2X1 HEADER_2X1
25	17	J34,J35,J36,J37,J38,J39, J40,J41,J42,J43,J44,J45, J46,J47,J48,J49,J50	STR3CMS STR3CMS

26	2	J72,J73	TESTPIN HEADER_1X1
27	3	J92,J93,J99	HEADER_3 HEADER_3X1
28	6	L1,L2,L3,L4,L5,L6	BEAD 1206
29	4	L7,L8,L9,L10	2.7uH 1206
30	1	L11	BEAD
31	1	OS1	OSCP OSCP
32	1	OS2	27MHz
33	1	P1	DBS15F DBS15F
34	2	P2,P3	MINIDIN MINIDIN
35	2	P4,P5	HEADER_13X2 HEADER_13X2
36	1	P6	CINCH_F CINCH_F
37	1	P7	PERITEL SCART
38	3	P8,P9,P10	PCI32 PCI32
39	1	P11	CONNECTOR_DB9 DB9MC
40	1	P12	HEADER_5X2 HEADER_5X2
41	2	P13,P14	HEADER_20X2 HEADER_20X2
42	1	P15	HEADER_17X2 HEADER_17X2
43	1	P17	ATX ATX
44	1	P18	HEADER_5 HEADER_5X1
45	1	P19	POWER12 POWER12
46	3	PA1,PA2,PA3	BUS62 BUS62
47	3	PB1,PB2,PB3	BUS36 BUS36
48	4	Q1,Q2,Q3,Q4	2N2907A SOT23
49	2	Q5,Q6	2N3904 SOT23
50	1	Q7	2N3906 SOT23
51	31	R1,R3,R4,R5,R6,R7,R8, R9,R10,R11,R12,R13,R14, R15,R16,R17,R18,R19,R20, R21,R22,R23,R24,R25,R26, R27,R28,R29,R30,R31	33 0805
52	11	R32,R33,R34,R35,R36,R37, R38,R39,R40,R41,R42	1K 0805
53	22	R44,R45,R51,R52,R53,R55, R56,R57,R58,R59,R60,R61, R62,R80,R166,R167	4.7K 0805
54	1	R63	536_1% 0805
55	10	R64,R66,R67,R68,R69,R70, R71,R72,R73	22 0805
56	17	R65,R79,R81,R82,R83,R84, R85,R86,R87,R88,R89,R90, R91	0 0805
57	1	R92	1M 0805
58	7	R93,R94,R95,R96,R97,R98, R99	75_1% 0805
59	14	R100,R101,R102,R103,R104, R105,R106,R107,R108,R109, R110,R111,R112,R170	10K 0805
60	4	R113,R114,R115,R116	200 0805
61	5	R117,R118,R119,R120,R121	1.2K 0805
62	4	R122,R123,R124,R125	12 0805
63	4	R126,R127,R128,R129	1.8K 0805
64	4	R130,R131,R132,R133	8.2 0805
65	1	R134	3.3K 0805
66	7	R135,R136,R137,R138,R139, R140,R175	2.2K 0805
67	4	R141,R142,R143,R144	300 0805
68	1	R145	10M 0805
69	3	R146,R147,R148	100 0805
70	4	R149,R150,R151,R152	82 0805

71	6	R153,R154,R155,R163,R164, R165	150 0805
72	2	R156,R157	5.6K 0805
73	3	R158,R159,R174	220 0805
74	2	R160,R173	330 0805
75	2	R161,R162	8.2K 0805
76	1	R168	200
77	1	R169	82
79	64	RP1A,RP1B,RP1C,RP1D,RP2A,RP2B,RP2C,RP2D,RP3A,RP3B,RP3C,RP3D,RP4A,RP4B,RP4C,RP4D,RP5A,RP5B,RP5C,RP5D,RP6A,RP6B,RP6C,RP6D,RP7A,RP7B,RP7C,RP7D,RP29A,RP29B,RP29C,RP29D,RP30A,RP30B,RP30C,RP30D,RP31A,RP31B,RP31C,RP31D,RP32A,RP32B,RP32C,RP32D,RP33A,RP33B,RP33C,RP33D,RP34A,RP34B,RP34C,RP34D,RP35A,RP35B,RP35C,RP35D,RP36A,RP36B,RP36C,RP36D,RP37A,RP37B,RP37C,RP37D	CRA4 22
80	16	RP8A,RP8B,RP8C,RP8D,RP9A,RP9B,RP9C,RP9D,RP10A,RP10B,RP10C,RP10D,RP11A,RP11B,RP11C,RP11D	CRA4 2.2K
81	32	RP12A,RP12B,RP12C,RP12D,RP13A,RP13B,RP13C,RP13D,RP14A,RP14B,RP14C,RP14D,RP15A,RP15B,RP15C,RP15D,RP16A,RP16B,RP16C,RP16D,RP17A,RP17B,RP17C,RP17D,RP18A,RP18B,RP18C,RP18D,RP21A,RP21B,RP21C,RP21D	CRA4 8.2K
82	8	RP19A,RP19B,RP19C,RP19D,RP20A,RP20B,RP20C,RP20D	CRA4 5.6K
83	42	RP22A,RP22B,RP22C,RP22D,RP23A,RP23B,RP23C,RP23D,RP26A,RP26B,RP26C,RP26D,RP27A,RP27B,RP27C,RP27D,RP38A,RP38B,RP38C,RP38D,RP39A,RP39B,RP39C,RP39D,RP40A,RP40B,RP40C,RP40D,RP41A,RP41B,RP41C,RP41D,RP42,RP43,RP43C,RP43D,RP44A,RP44B,RP44C,RP44D,RP45,RP46	CRA4 4.7K
84	8	RP24A,RP24B,RP24C,RP24D,RP25A,RP25B,RP25C,RP25D	CRA4 330
85	4	RP28A,RP28B,RP28C,RP28D	CRA4 150
86	2	SW1,SW2	SW_PUSHBUTTON SWCI
87	1	U1	SIP1 BGA388
88	6	U2,U3,U4,U5,U6,U7	74F245 SO20
89	4	U8,U9,U10,U11	SIMM-36BIT SIMM72
91	1	U13	LF33 DPAK
92	1	U14	MINIDIN4 MINIDIN4
93	4	U15,U16,U17,U18	74F153 SO16
94	1	U19	74F138 SO16

95	1	U20	PC87306VUL PQFP160
96	2	U21A,U21D	74F32 SO14
97	4	U22,U23,U24,U25	74F74V SO14
98	1	U26	M27C2001 DIP32
99	1	U27	UM8667 SSOP48
100	4	U28A,U28B,U28C,U28D	74F00 SO14
101	4	U29A,U29B,U29C,U29D	74LS14 SO14
102	1	U30	74F32V SO14
103	1	U31	74LS14V SO14
104	1	U32	LT1085CT TO220
105	1	U33	74F125
106	1	U34	74LS14
107	1	Y1	14.3MHz HC49U
108	1	Y2	32KHz KF38

MAY NOT BE INSTALLED

C13,C22,C54,C71

L6

OS1

U15

DO NOT INSTALL

R2,R46,R47,R48,R49,R50,R74,R54,R75,R76,R77,R78,R171

U12

STR3CMS

Assemble all in [2-3] position except J36 and J37 ([1-2])

WIRING MODIFICATIONS

4.4 How to design for both STPC Client and STPC Consumer

This chapter describes how to make a board design for both STPC Client and STPC Consumer (A.N.H97001-Release 1.2-24/12/97).

4.4.1 Differences between STPC Client and STPC Consumer

4.4.1.1 Functionnal differences.

The STPC Client is historically the first device of STPC Family.
The STPC Consumer's main external difference with its predecessor is the analog TV output instead of a digital one.

TABLE 37. STPC Client and STPC Consumer functionnal differences

STPC Client	STPC Consumer
Needs an oscillator for internal clocks generation	Needs a quartz for internal clocks generation
Digital TV output	Analog TV output
10 reserved pins	Only 1 reserved pin

4.4.1.2 Pinout differences.

For technical reasons, 49 signals were changed or moved from STPC Client to STPC Consumer on which 10 are just renamed.

TABLE 38. STPC Client and STPC Consumer pinout differences

STPC	Client	STPC	Consumer	
Pin	SignalName	Pin	SignalName	Comment
AF10	TV_YUV[0]			Removed
AC10	TV_YUV[1]			Removed
AE11	TV_YUV[2]			Removed
AD10	TV_YUV[3]			Removed
AF11	TV_YUV[4]			Removed
AE12	TV_YUV[5]			Removed
AF12	TV_YUV[6]			Removed
AD11	TV_YUV[7]			Removed
AD9	VTV_BT#	AD9	ODD_EVEN	Renamed
AE10	VTV_HSYNC	AE10	VCS	Renamed
B4	ST[0]			Removed
D5	ST[1]			Removed
A4	ST[2]			Removed

TABLE38.STPCClientandSTPCConsumerpinoutdifferences

STPC	Client	STPC	Consumer	
C5	ST[3]			Removed
B3	ST[4]			Removed
C4	ST[5]	C5	SPKRD	Renamed&Moved
A3	ST[6]			Removed
C7	CLKDEL[0]			Removed
B5	CLKDEL[1]			Removed
A5	CLKDEL[2]			Removed
AF5	DCLK_DIR			Removed
D24	PCI_INT[0]	A5	PCI_INT[0]	Moved
C26	PCI_INT[1]	C6	PCI_INT[1]	Moved
A25	PCI_INT[2]	B4	PCI_INT[2]	Moved
B24	PCI_INT[3]	D5	PCI_INT[3]	Moved
AD14	VIDEO_CLK	AC12	VCLK	Renamed&Moved
AE13	VIDEO_D[0]	AE13	VIN[0]	Renamed
AC12	VIDEO_D[1]	AD14	VIN[1]	Renamed&Moved
AD12	VIDEO_D[2]	AD12	VIN[2]	Renamed
AE14	VIDEO_D[3]	AE14	VIN[3]	Renamed
AC14	VIDEO_D[4]	AC14	VIN[4]	Renamed
AF14	VIDEO_D[5]	AF14	VIN[5]	Renamed
AD13	VIDEO_D[6]	AD13	VIN[6]	Renamed
AE15	VIDEO_D[7]	AE15	VIN[7]	Renamed
AF15	XTALI	A3	XTALI	Moved
AE16	XTALO	C4	XTALO	Moved
W4	VDD_GCLK_PLL	AD19	VDD_GCLK_PLL	Moved
AB1	VDD_DCLK_PLL	AF13	VDD_DCLK_PLL	Moved
C6	OSC14M	AF8	OSC14M	Moved
AD8	DDC[0]	C7	DDC[0]	Moved
AF8	DDC[1]	B5	DDC[1]	Moved
AD5	DCLK	AF9	DCLK	Moved
AC5	GCLK2X	AF15	GCLK2X	Moved
AF9	HSYNC	AC5	HSYNC	Moved
AE9	VSNC	AD5	VSNC	Moved
AC9	COMP	AF5	COMP	Moved
AF13	VDD	AB1	VDD	Moved
AD19	VDD	W4	VDD	Moved
AD7	VREF	AD7	VREF_DAC	Renamed
		AE16	VSS	New
		AF10	RED_TV	New
		AC10	GREEN_TV	New

TABLE38.STPCClientandSTPCConsumerpinoutdifferences

STPC	Client	STPC	Consumer	
		AF11	BLUE_TV	New
		AD11	CVBS	New
		AD8	IREF1_TV	New
		AE11	IREF2_TV	New
		AE9	VREF1_TV	New
		AD10	VREF2_TV	New
		AF12	VDDA_TV	New
		AE12	VSSA_TV	New
		A4	RTCAS#	New
		AC9	ZWS#	New
		B3	SCAN_ENABLE	New

4.4.2 Signalmultiplexing

4.4.2.1 Constraints.

Thereareseveralwaystodesignaboardwhichacceptbothcomponents.

TABLE39.Possiblechoiceswhenmultiplexingsignals

Solution	Advantages	Drawbacks
2footprints	simpleschematics simpleBOM flexible(ifsocket)	increaseboardsize+ increaseroutingcomplexity+ longernets+ cost
1footprint Multiplexors	spaceonboard simpleBOM flexible(ifsocket)	complexschematics increaseboardsize increaseroutingcomplexity longernets netdelayandloadingaremodified cost
1footprint 0ohmsresistors DifferentBOMs	spaceonboard+ systemspeedcost	complexschematics+ notflexible twoBOMs

Forourevaluationboard,forexample,wewantedasmallboardwithlowpriceandthebest performance,wechosetouse the0ohmresistors solution.

4.4.2.2 Solution

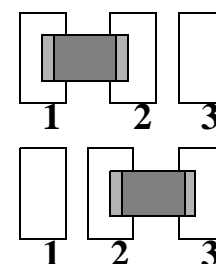
TABLE40.SolutionusingnullresistorsasmultiplexorsandmultipleBOMs.

Pin	Signal[Client] Signal[Consumer]	Connecting component	SignaloftheBoard
D26,C26,A25,B24	PCI_INT[0:3] Unconnected	0ohm -	PCI_INT[0:3] -
C7,B5	CLKDEL[0:1] DDC[0:1]	4K7pullup 0ohm	3.3V DDC[0:1]
A5	CLKDEL[2] PCI_INT[0]	4K7pullup 0ohm	3.3V PCI_INT[0]
B4,D5	ST[0:1] PCI_INT[2:3]	4K7pullup 0ohm	3.3V PCI_INT[2:3]
A4	ST[2] RTCAS#	4K7pullup 0ohm	3.3V RTCAS#
C5	ST[3] SPKRD	4K7pullup 0ohm	3.3V SPKRD
B3	ST[4] SCAN_ENABLE	- 4K7pulldown	- GND
C4	ST[5] XTALO	0ohm 0ohm	SPKRD XTALO
A3	ST[6] XTALI	- 0ohm	- XTALI
AD14	VIDEO_CLK VIN[1]	0ohm 0ohm	VIDEO_CLK VIN[1]
AC12	VIDEO_D[1] VCLK	0ohm 0ohm	VIDEO_D[1] VCLK
AD8	DDC[0] IREF1_TV	0ohm 0ohm	DDC[0] IREF1_TV
AF8	DDC[1] OSC14M	0ohm 0ohm	DDC[1] 3.3V
AF15	XTALI GCLK2X	0ohm -	XTALI -
AE16	XTALO VSS	0ohm 0ohm	XTALO GND
C6	OSC14M PCI_INT[1]	0ohm 0ohm	OSC14M PCL_INT[1]
W4	VDD_GCLK_PLL VDD	Wire Wire	3.3V 3.3V
AB1	VDD_DCLK_PLL VDD	Wire Wire	3.3V 3.3V
AD19	VDD VDD_GCLK_PLL	Wire Wire	3.3V 3.3V
AF13	VDD VDD_DCLK_PLL	Wire Wire	3.3V 3.3V
AD5	DCLK VSYNC	0ohm 0ohm	DCLK VSYNC

TABLE 40. Solution using null resistors as multiplexors and multiple BOMs.

Pin	Signal[Client] Signal[Consumer]	Connecting component	Signal of the Board
AC5	GCLK2X HSYNC	- 0ohm	- HSYNC
AF9	HSYNC DCLK	0ohm 0ohm	HSYNC DCLK
AF5	DCLK_DIR COMP	4K7pulldown 0ohm	GND COMP
AC9	COMP ZWS#	0ohm 0ohm	COMP ZWS#
AE9	VSYNC VREF1_TV	0ohm 0ohm	VSYNC VREF1_TV
AF10	TV_YUV[0] RED_TV	0ohm 0ohm	TV_YUV[0] RED_TV
AC10	TV_YUV[1] GREEN_TV	0ohm 0ohm	TV_YUV[1] GREEN_TV
AE11	TV_YUV[2] IREF2_TV	0ohm 0ohm	TV_YUV[2] IREF2_TV
AD10	TV_YUV[3] VREF2_TV	0ohm 0ohm	TV_YUV[3] VREF2_TV
AF11	TV_YUV[4] BLUE_TV	0ohm 0ohm	TV_YUV[4] BLUE_TV
AE12	TV_YUV[5] VSSA_TV	0ohm 0ohm	TV_YUV[5] AGND
AF12	TV_YUV[6] VDDA_TV	0ohm 0ohm	TV_YUV[6] Analog3.3V
AD11	TV_YUV[7] CVBS	0ohm 0ohm	TV_YUV[7] CVBS
AE10	VTV_HSYNC VCS	0ohm 0ohm	VTV_HSYNC VCS
AD9	VTV_BT# ODD_EVEN	0ohm 0ohm	VTV_BT# ODD_EVEN

The configuration 0 ohm twice in the same 'connecting component' box is done using a 0 ohm multiplexor. This is achieved using a 3-pad SMD footprint where you put a 0 ohm resistor in the one of the two possible locations. Using a 0805 SMD resistor, this assumes a very small multiplexor with good electrical characteristics.



In addition to this table, we must take into account the external STV0119 used with the ST PC Client. If it is always on the board, TV_YUV[0:7], VTV_HSYNC and VTV_BT# must be connected through the 0 ohm resistors in the table. If it is not installed with the ST PC Consumer (recommended choice) then the number of 0 ohm resistors can be reduced.

For analog signals with electrical constraints like voltage references and current references, it is possible to duplicate the discrete components connected and to place one of each set near the corresponding component.

For example, capacitors and resistors on VREFxx and IREFxx lines can be duplicated. One set is assembled only when the STV0119 is on board (STPCC Client), the other set is assembled only when the STPCC Consumer is present.

4.4.3 Example

see schematics in this document or download the up to date Reference Design (ST/NVG intranet webpage).

4.4.4 Application Note History

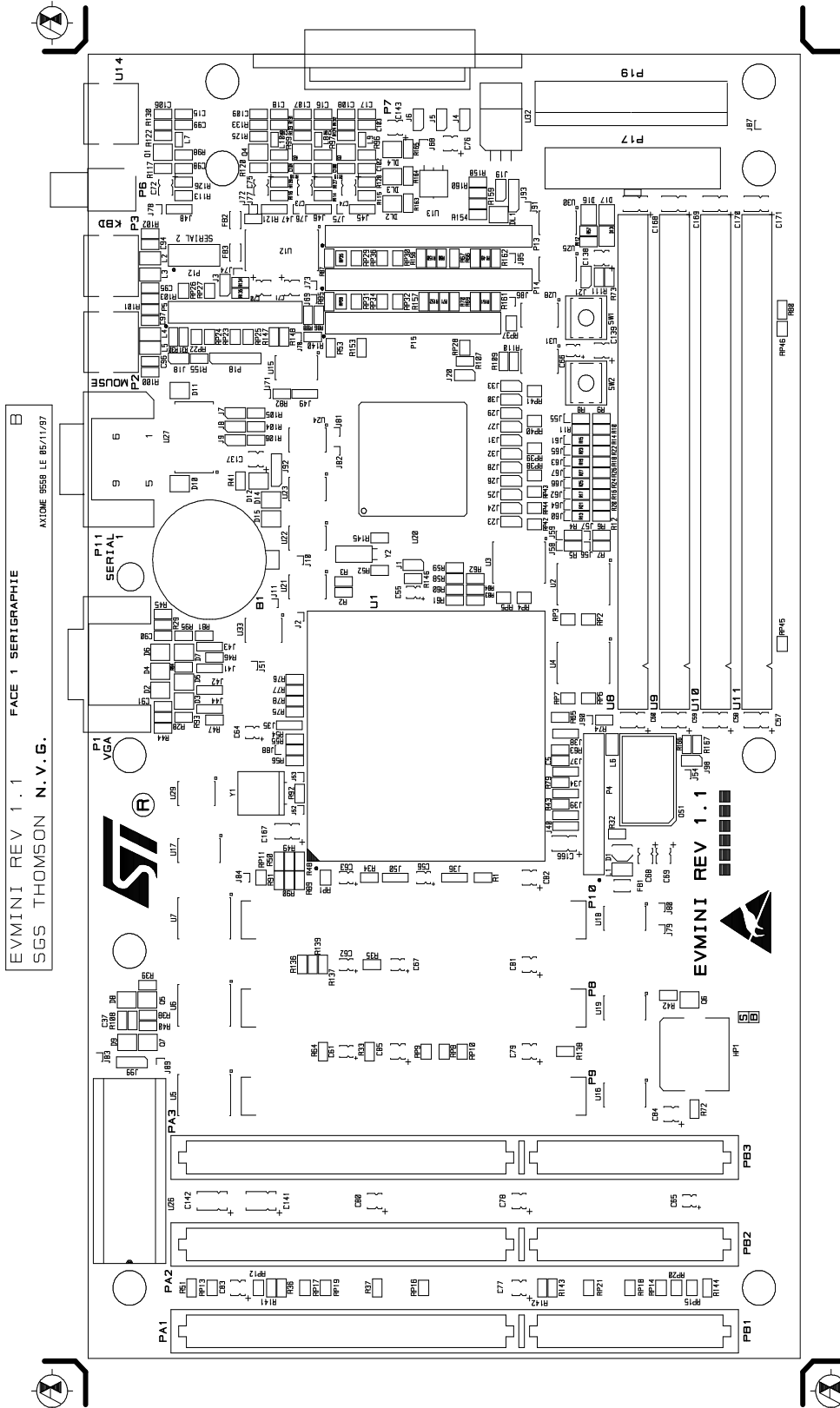
Release 1.0: First Release.

Release 1.1: Updated due to improved STPCC Consumer pinout.

Release 1.2: Updated due to external DCLK Video Clock (27MHz).

4.5 PCB

4.5.1 Silkscreen



4.6 Electrical Specifications

The Power Supply used to power this board must have the characteristics detailed in the following table.

TABLE 41. Power Supply Characteristics

Voltage	Precision
+5V	+/-250mV
+12V	+/-600mV
-5V	+/-500mV
-12V	+/-1.2V
+3.3V	+/-300mV

5. Motherboard Software Specifications.

5.1 System Address Map:

This section describes the mapping of the CPU memory and IO address spaces. Also covered in this section are the PCI configuration space mapping

5.1.1 Memory Address Map.

TABLE 42. Memory Address Map

Address Range (Dec)	Address Range (Hex)	Size	Description
1024K-16984K	100000-1000000	15960K	Extended Memory
896K-1024K	0E0000-0FFFFFFF	128K	System Bios
768K-800K	0C0000-0C7FFFFF	32K	Graphic Bios
736K-768K	0B8000-0BFFFFF	32K	Monochrome Text Memory
704K-736K	0B0000-0B7FFF	32K	Color Text Memory
640K-704K	0A0000-0AFFFFF	64K	“Graphic” Memory
0K-640K	0-9FFFFF	640K	Conventional Memory

5.1.2 IOAddressMAP

The system chip-set implements a number of registers in IO address space. These registers occupy the following map in the IO space.

TABLE 43. IOAddressMap

Address Range (Hex)	Size (Hex)	Description
0000-000F	16 Bytes	DMA Controller 1 (8237)
0020-0021	2 Bytes	Interrupt Controller 1 (8259)
0022-0023	2 Bytes	ST486 Specific Registers
0040-0043	4 Bytes	Timer Controller (8254)
0060	1 Bytes	Keyboard Controller Data Byte
0061	1 Byte	NMI, Speaker Control
0064	1 Byte	Kbd Ctlr, CMD, STAT Byte
0070, bit 7	1 bit	Enable
0070, bit 6:0	7 bits	Real Time Clock Address
0078	1 Byte	General Purpose I/O
0080-008F	16 Bytes	DMA Page Registers
00A0-00A1	2 Bytes	Interrupt Controller 2 (8259)
00C0-00DE	31 Bytes	DMA Controller 1 (8237)
00F0	1 Byte	Reset Numeric Error
0102	1 Byte	VGA Setup Register
0170-0177	8 Bytes	Secondary IDE Channel
01F0-01F7	8 Bytes	Primary IDE Channel
0278-027B	4 Bytes	Parallel Port 2 (Bidir)
02F8-02FF	8 Bytes	Serial Port 2
0378-037F	8 Bytes	Parallel Port 1
03B4, 03B5, 03BA	3 bytes	VGA Registers
03D4, 03D5, 03DA	3 Bytes	VGA Registers
03C0-03CF	16 Bytes	VGA Registers
03F0-03F5	6 Bytes	Floppy Controller Registers
03F6	1 Byte	IDE Command Port
03F7 (Write)	1 Byte	Floppy Command Port
03F7, bit 7	1 bit	Floppy Disk Change
03F7, bits 6:0	7 bits	IDE Status Port
03F8-03FF	8 Bytes	Serial Port 2
0CF8	1 Byte	PCI Configuration Address Register
0CFC-0CFF	8 Bytes	PCI Configuration Data Registers
04E8	1 Byte	VGA Add-in mode enable Register
C000-C0FF	256 Bytes	PCI Configuration Registers

5.2 InterruptsandDMAChannels

TABLE44.IRQChannels

IRQ	SystemResource
NMI	ParityError
0	Reserved,IntervalTimer
1	Reserved,KeyboardbufferFull
2	Reserved,CascadeInterruptfromInterrupt Controller2
3	SerialPort2
4	SerialPort1
5	ParallelPort2(P10)
6	Floppy
7	ParallelPort1
8	RealTimeClock
9	Useravailable(video)
10	Useravailable
11	Useravailable
12	PS/2MousePort
13	Reserved,Mathcoprocessor
14	IDE
15	Useravailable/IDE

TABLE45.DMAChannels

DMA	DataWidth	SystemResource
0	8bits	Useravailable
1	8bits	Useravailable
2	8bits	Floppy
3	8bits	ParallelPort
4		Reserved,CascadeChannel
5	16bits	IDEController
6	16bits	UserAvailable
7	16bits	UserAvailable

6. DocumentHistory.

Release0.9:7/9/98-FirstRelease